"SYNTEC" CMOS Logic Array Main series parameters and characteristics

The integrated circuits are produced according to CMOS-technology with poly gates and are almost compatible with series 74HC, 74AC).
Logic Array KP1580XM3 has small capacity, high load capability and operating speed, low power consumption. These chip characteristics and the constructional peculiarities (not more than 16 pins) give an opportunity to use this chip as an indicators' control integrated circuit in many spheres of application. The most promising of them are the indication system with higher indicator brightness, the system with indicator multiplex switching-on, the system with many-colored indicators' switching-on, the indication system with connection to high-speed computer port, indicators of light-emitting diode matrix.

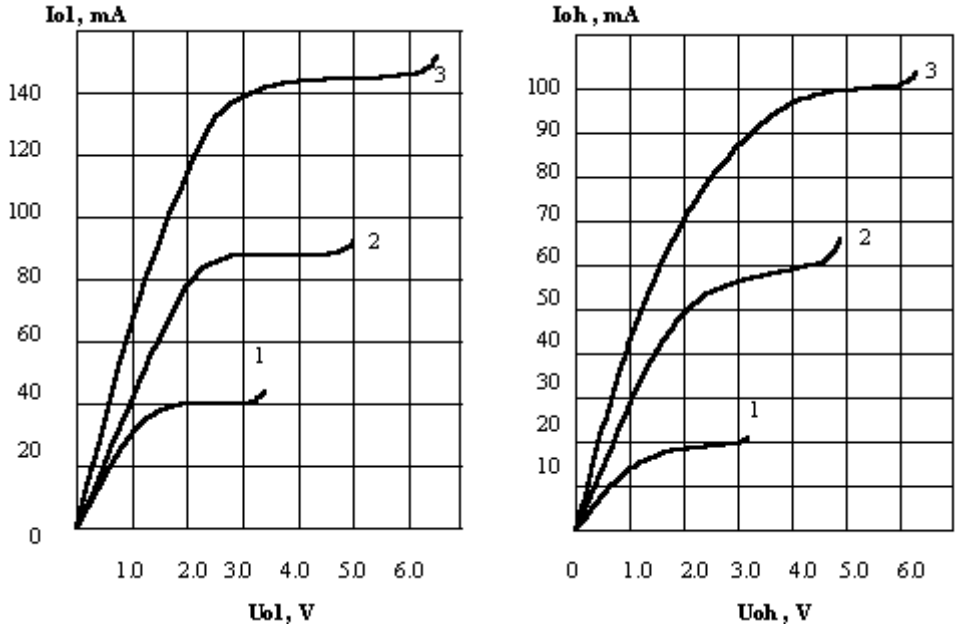
Static and dynamic parameters of integrated circuits used in Logic Arrays

Parameter Name	Sign	Norm		Measurement mode				Temperature,°C
		min	max	Ucc, B	Uil, B	Uih, B	Io, мА	
1. Max. output low-level voltage, V	Uol		0.10	3.0	0.6	2.10	0.02	-10, +25, +85
				4.5	0.9	3.15		
				6.0	1.2	4.20		
			0.26	4.5	0.9	3.15	4.0	+25
			0.40					-10, +85
2. Min. output high-level voltage, V	Uoh	2.90		3.0	0.6	2.10	0.02	-10, +25, +85
		4.40		4.5	0.9	3.15		
		5.90		6.0	1.2	4.20		
		3.98		4.5	0.9	3.15	4.0	+25
		3.60						-10, +85
3. Input low- and high-level current, mkA	I_{il}		0.1	6.0	0.0	6.0	-	+25
	I_{ih}		1.0					-10, +85
4. Leakage low- and high-level current in the 3d state, mkA	I_{ozl}		0.5	6.0	0.0	6.0	-	+25
	I_{ozh}		5.0					-10, +85
5. Consumption current, mkA	Icc		1.0	6.0	0.0	6.0	-	+25
			10.0					-10, +85
6. Turn-on and turn-off delay time, ns/inverter	t_{plh}		5.0	4.5	0.0	4.5	-	+25
	t_{phl}		10.0					-10, +85

Permissible limit and limit Logic Array parameters

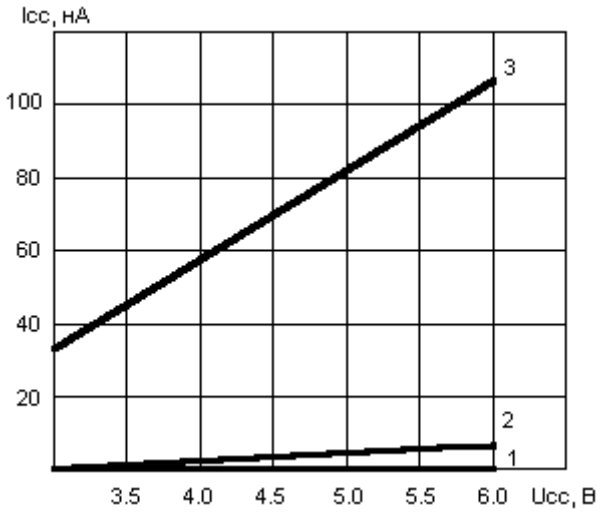
Parameter Name	Sign	Operating mode norm			
		permissible limit		limit	
		min	max	min	max
1. Supply voltage, V	Ucc	3.0	6.0	-0.5	9.0
2. Input low-level voltage, V	U_{il}		0.2 Ucc	-0.5	
3. Input high-level voltage, V	U_{ih}	0.7 Ucc			Ucc+0.5
4. Output current, mA	Io		30		50
5. Average current through Vcc (power supply) and GND (common), mA	Icc		50		100
6. Max.duration front and edge of the input signal, ns	tr				500
7. Power dissipation, mW	P				300
8. Max. load capacitance, pF	C_{max}				500
9. Temperature range, °C	T	-10	+85	-60	+100

Current-voltage characteristics of Logic Array outputs



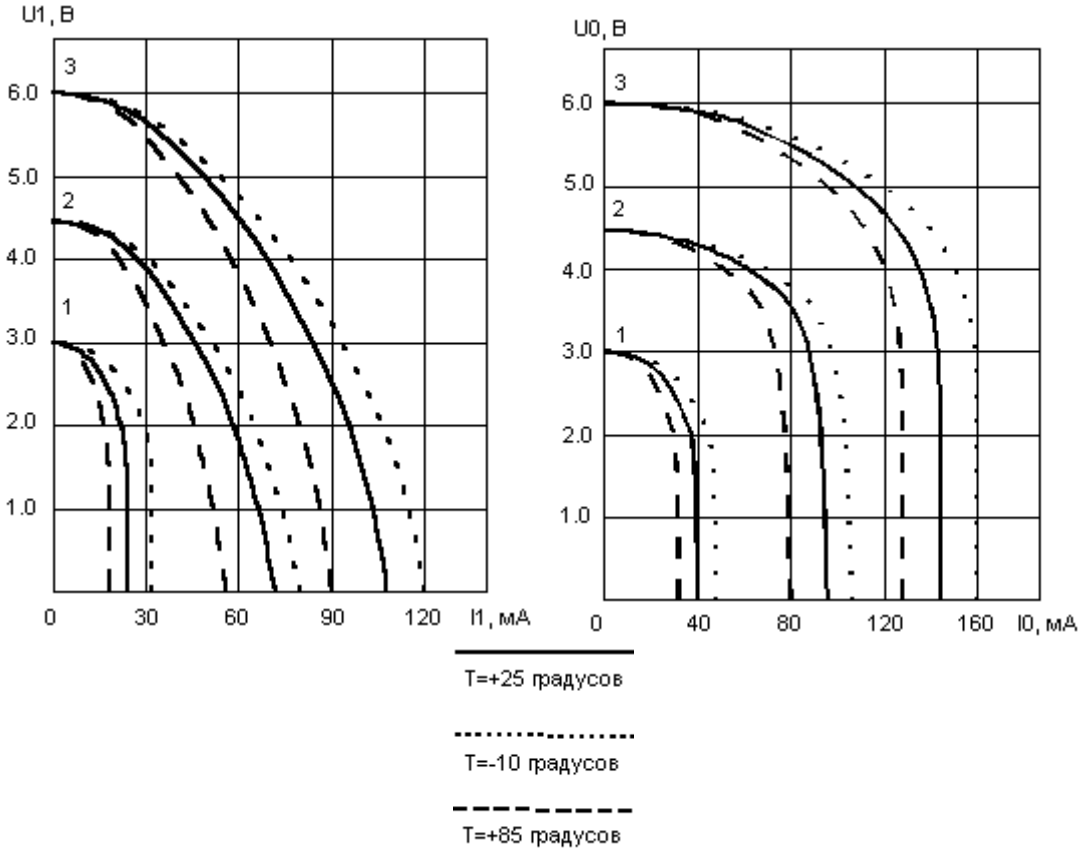
а) - n-channel integrated circuit output; б) - p-channel integrated circuit output;
1 - voltage Ugs=3,0 V ; 2 - voltage Ugs=4,5 V ; 3 - voltage Ugs=6,0 V

Supply voltage dependence of supply static current



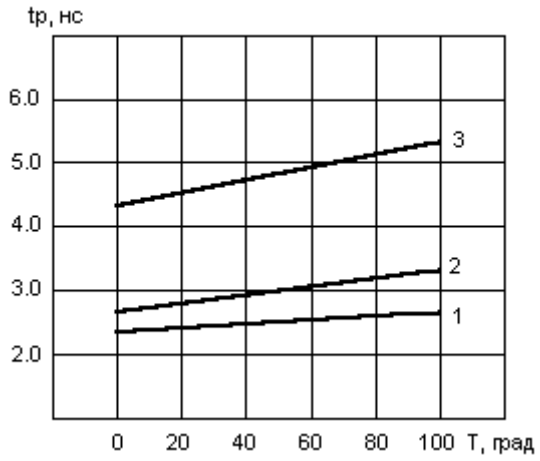
1 - at T= - 10 °C; 2 - at T= + 25 °C; 3 - at T= + 85 °C

Load capacity in "1"- state and "0"-state



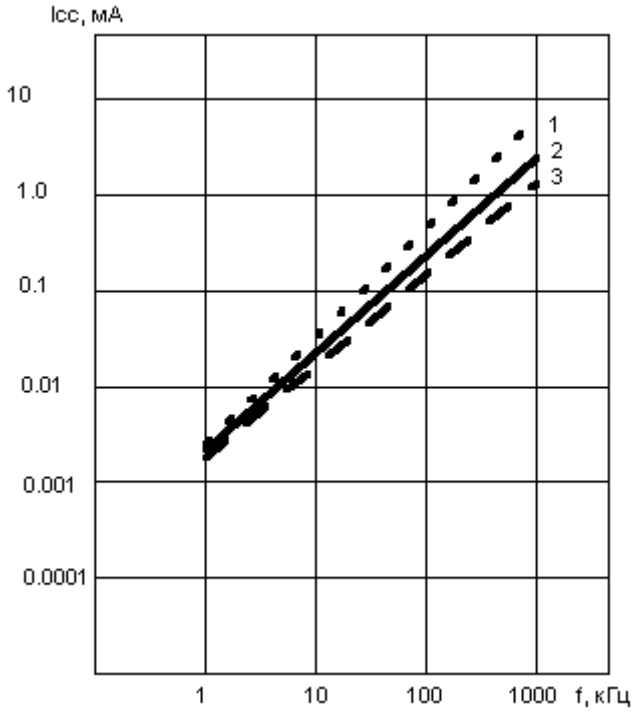
1 - voltage Ugs=3,0 V; 2 - voltage Ugs=4,5 V; 3 - voltage Ugs=6,0 V

Lag time of 1 invertor spreading



1 - supply voltage 6,0 V; 2 - supply voltage 4,5 V; 3 - supply voltage 3,0 V

Frequency dependence of max. dynamic supply current



1 - temperature 85° C; 2 - temperature 25° C; 3 - temperature -10° C